CLAIMS

What is claimed is:

1. A system for digital signal processing within an adaptive computing engine, the system comprising:

a mini-matrix, the mini-matrix comprising a set of composite blocks, each composite block capable of executing a predetermined set of instructions;

a sequencer for controlling the set of composite blocks and directing instructions among the set of composite blocks based on a dataflow graph;

a data network for transmitting data to and from the set of composite blocks and to the sequencer; and

a status network for routing status word data resulting from instruction execution in the set of composite blocks.

2. The system of claim 1 wherein each composite block is capable of executing a set of atomic instructions.

3. The system of claim 2 wherein the set of atomic instructions further comprises a set of n-bit instructions, including arithmetic, logic, and multiply-accumulate and shift instructions.

4. The system of claim 3 wherein the set of n-bit instructions further comprises a set of 16-bit instructions.

5. The system of claim 1 wherein each composite block further comprises first and second register files coupled to a multiplier-ALU-shifter, the multiplier-ALU-shifter further coupled to an accumulator register file.

6. The system of claim 5 wherein the first and second register files store data received from the data network as operands and the multiplier-ALU-shifter performs an instruction and outputs results to the data network.

7. The system of claim 1 wherein each composite block further comprises a status register file for storing status words received from the status network.

8. The system of claim 7 wherein the status network routes status words data independently of results transmitted on the data network.

9. The system of claim 1 wherein the sequencer transmits instruction words for the mini-matrix, the instruction words subdivided into instruction fields for parallel performance of computation, input, output, and control instructions in the mini-matrix.

10. A method for digital signal processing within an adaptive computing engine, the system comprising:

designating a set of composite blocks as a mini-matrix, each composite block capable of executing a predetermined set of instructions;

utilizing a sequencer for controlling the set of composite blocks and directing instructions among the set of composite blocks based on a dataflow graph;

providing a data network for transmitting data to and from the set of composite blocks and to the sequencer; and

providing a status network for routing status word data resulting from instruction execution in the set of composite blocks.

11. The method of claim 10 wherein each composite block is capable of executing a set of atomic instructions.

12. The method of claim 11 wherein the set of atomic instructions further comprises a set of n-bit instructions, including arithmetic, logic, and multiply-accumulate and shift instructions.

13. The method of claim 12 wherein the set of n-bit instructions further comprises a set of 16-bit instructions.

14. The method of claim 10 further comprising providing first and second register files coupled to a multiplier-ALU-shifter, the multiplier-ALU-shifter further coupled to an accumulator register file in each composite block.

15. The method of claim 14 further comprising storing received data from the data network in the first and second register files as operands, performing an instruction with the multiplier-ALU-shifter, and outputting results to the data network.

16. The method of claim 10 further comprising storing status words received from the status network in a status register in the composite block.

17. The method of claim 16 further comprising routing status words on the status network independently of results data transmitted on the data network.

18. The method of claim 10 further comprising transmitting instruction words from the sequencer for the mini-matrix, the instruction words subdivided into instruction fields for parallel performance of computation, input, output, and control instructions in the mini-matrix.

19. A system for digital signal processing in an adaptive computing engine, the system comprising:

a set of four computation blocks designated as a mini-matrix, each of the four computation blocks comprising:

first and second register files for storing operand data;

a multiplier-ALU-shifter coupled to the first and second register files for performing an instruction and outputting results data; and

an accumulator register file coupled to the multiplier-ALU-shifter for storing accumulation data; and

a sequencer for controlling the set of four composite blocks and directing instructions among the set of four composite blocks based on a dataflow graph.

20. The system of claim 19 further comprising a data network for transmitting data to and from the set of four composite blocks and to the sequencer.

21. The system of claim 20 further comprising a status network for routing status words resulting from instruction execution in the set of four composite blocks.

22. The system of claim 19 wherein each composite block is capable of executing a set of 16-bit atomic instructions, including arithmetic, logic, and multiply-accumulate and shift instructions.

23. The system of claim 21 wherein the status network routes status words independently of results data transmitted on the data network.

24. The system of claim 20 wherein the sequencer transmits instruction words for the mini-matrix, the instruction word data subdivided into instruction fields for parallel performance of computation, input, output, and control instructions in the mini-matrix.